디지털 공학 (MEC520)
Final Examination

Spring, 2008

1. Design a 4-input priority encoder with input D0 (the Lowest Significant Bit) having the highest priority and input D3 (the Highest Significant Bit) having the lowest priority. Assume that x, y are outputs, and y is the Lowest Significant Bit. Don't care the outputs when all 4-inputs are zero. (20pt)

2. Design the negative edge triggered synchronous 3-bit binary counter using T flip-flops and one input *x*, count up when *x=0*, and count down when *x=1*. (20pt)

3. Design a negative edge triggered synchronous sequential circuit with two JK flip-flops A and B, and one input *x*. when *x*=0, the state of the circuit remains the same. When *x*=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeated. (20pt)

4. Design a positive edge triggered synchronous sequential circuit with two T flip-flops A and B and two inputs x and y. if x=0, the circuit remains in the same state regardless of the value of y. when x=1 and y=1, the circuit goes through the state transitions form 00 to 01 to 10 to 11 back to 00, and repeats. When x=1 and y=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeat. (20pt)

5. Obtain the input Boolean functions for a synchronous counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use JK flip-flops. And obtain the next number when it start at 3, 5 or 7 (20pt)

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