디지털 공학 (MEC520)
Final Examination

Spring, 2010

1. Implement the following Boolean function with a 4 x 1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D. These values are obtained by expressing F as a function of C and D for each of the four cases when AB=00, 01, 10 and 11. These functions may have to be implemented with external gates. (20pt)

$$F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$$

2. Design a positive edge triggered synchronous sequential circuit with two JK flip-flops A and B and two inputs x and y. if x=0, the circuit remains in the same state regardless of the value of y. when x=1 and y=1, the circuit goes through the state transitions form 00 to 01 to 10 to 11 back to 00, and repeats. When x=1 and y=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeat. (20pt)

3. Following circuit shows serial adder with shift registers and D flip-flop. In this figure D flip-flop was used for storing the carry. Convert the circuit by using the JK flip-flop for storing the carry and by expressing the sum with external gates. (20pt)

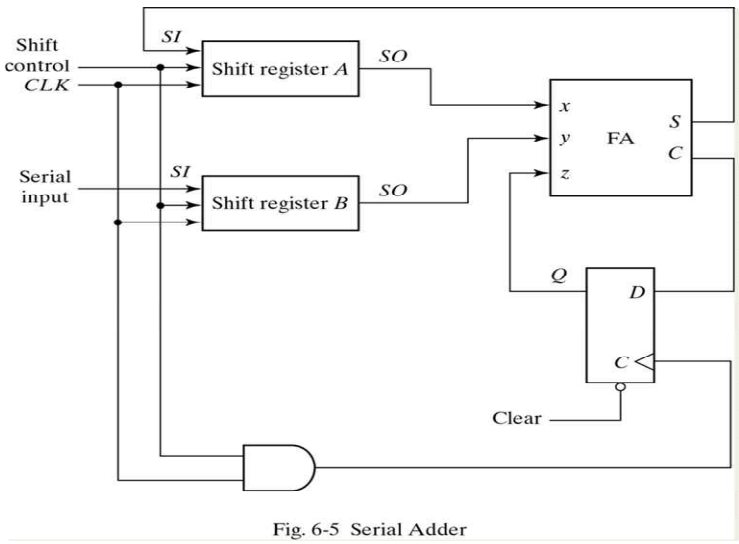

Fig. 6-5 Serial Adder

4. Fill out two blanks with proper VHDL codes. (20pt)

5. Obtain the input Boolean functions for a synchronous counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use JK flip-flops. And obtain the next number when it start at 3, 5 or 7 (20pt)

Adder

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
ENTITY EX_2_1_V IS
	PORT(
	A : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
	B : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
	C : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
	S : OUT STD_LOGIC_VECTOR(1 DOWNTO 0 ) );
END EX_2_1_V;
ARCHITECTURE HB OF EX_2_1_V IS
	SIGNAL TMP : STD_LOGIC_VECTOR(2 DOWNTO 0);
BEGIN
	TMP <= (_____)
	C(1) <= TMP(2);
	C(0) <= A(0) AND B(0);
	S <= TMP(1 DOWNTO 0);
END HB;
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY EX_6_1_V IS
	PORT(
		SET, CLR, CLK : IN STD_LOGIC;
		(_____)
END EX_6_1_V;

ARCHITECTURE BH OF EX_6_1_V IS
BEGIN
PROCESS(SET, CLR, CLK)
BEGIN
	IF SET = '0' THEN
		Q <= "1111";
	ELSIF CLR = '0' THEN
		Q <= "0000";
	ELSIF (CLK'EVENT AND CLK ='1') THEN
		IF Q = "1001" THEN
			Q <= "0000";
		ELSE
			Q <= Q+1;
		END IF;
	END IF;
END PROCESS;

END BH;
```

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