```
library ieee;
use ieee.std_logic_1164.all;

entity keypad2 is
port(
    clk         : in std_logic;
    k_scan      : buffer std_logic_vector(2 downto 0);
    k_data      : in std_logic_vector(3 downto 0);
    seg_com     : out std_logic_vector(7 downto 0);
    seg_data    : out std_logic_vector(7 downto 0));
end keypad2;

architecture a of keypad2 is
signal sw_data1 : integer range 0 to 18;
begin
process(clk)
begin
    if clk'event and clk = '1' then
        case k_scan is
            when "000" => k_scan <= "001";
            when "001" => k_scan <= "010";
            when "010" => k_scan <= "100";
            when "100" => k_scan <= "001";
            when others => k_scan <= "000";
        end case;
    end if;
end process;

process(clk)
begin
    if clk'event and clk = '1' then
        case k_scan is
            when "001" =>
                    case k_data is
                        when "0001" =>  sw_data1 <= 1;
                        when "0010" =>  sw_data1 <= 4;
                        when "0100" =>  sw_data1 <= 7;
                        when "1000" =>  sw_data1 <= 16;
                        when others =>  sw_data1 <= 18;
                    end case;
            when "010" =>
                    case k_data is
                        when "0001" =>  sw_data1 <= 2;
                        when "0010" =>  sw_data1 <= 5;
                        when "0100" =>  sw_data1 <= 8;
                        when "1000" =>  sw_data1 <= 0;
                        when others =>  sw_data1 <= 18;
                    end case;
            when "100" =>
                    case k_data is
                        when "0001" =>  sw_data1 <= 3;
                        when "0010" =>  sw_data1 <= 6;
                        when "0100" =>  sw_data1 <= 9;
                        when "1000" =>  sw_data1 <= 17;
                        when others =>  sw_data1 <= 18;
                    end case;
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            when others => sw_data1 <= 18;
        end case;
    end if;
end process;

process(clk)
begin
if clk'event and clk = '1' then
case sw_data1 is
    when 0 =>
        seg_data <= "11111100";
    when 1 =>
        seg_data <= "01100000";
    when 2 =>
        seg_data <= "11011010";
    when 3 =>
        seg_data <= "11110010";
    when 4 =>
        seg_data <= "01100110";
    when 5 =>
        seg_data <= "10110110";
    when 6 =>
        seg_data <= "10111110";
    when 7 =>
        seg_data <= "11100000";
    when 8 =>
        seg_data <= "11111110";
    when 9 =>
        seg_data <= "11100110";
    when 10 =>
        seg_data <= "11101110";
    when 11 =>
        seg_data <= "00111110";
    when 12 =>
        seg_data <= "10011100";
    when 13 =>
        seg_data <= "01111010";
    when 14 =>
        seg_data <= "10011110";
    when 15 =>
        seg_data <= "10001110";
    when 16 =>
        seg_data <= "10000000";
    when 17 =>
        seg_data <= "00010000";
    when 18 =>
        seg_data <= "00000000";
    when others =>
        seg_data <= "00000000";
end case;
end if;
end process;

seg_com <= "01111111";

end a;
```